CLAIMS

What is claimed is:

1. A method, comprising:

accessing data cache for data in response to a request for the data, the request received from an instruction source;

waiting for the data to be retrieved from memory if the data is not located in the data cache; and

receiving an early data ready indication at a resource scheduler, the early data ready indication being received prior to receiving a data ready indication referring to the data being ready to be retrieved from the memory.

2. The method of claim 1, further comprising:

receiving the data ready indication; and

filling the data cache with the data.

3. The method of claim 1, wherein the waiting for the data comprises:

inserting the request into the resource scheduler if the data is not located in the data cache; and

saving the request in the resource scheduler to wait for the data to be retrieved from the memory.

4. The method of claim 2, further comprising:

accessing the data cache with the request while the data cache is being filled with the data; and

meeting the request with the data from the data cache.

5. The method of claim 1, further comprises replaying the request to continue to snoop the data cache for the data, the replaying comprising repeating the request through the data cache for a given number of times.

6. The method of claim 1, wherein the request comprises at least one of an instruction and a load micro-operation.

7. The method of claim 1, wherein the data cache is coupled with an execution unit, the data cache comprising a first level cache (FLC) and a second level cache (SLC).

8. The method of claim 1, wherein the resource scheduler is coupled with a bus interface unit to receive the early data ready indication from a memory controller, the resource scheduler comprises a rescheduled request queue (RRQ).

9. The method of claim 1, wherein the memory controller is coupled with the bus interface unit via a front side bus.

10. A method, comprising:

detecting readiness of data one or more bus clocks prior to data being ready to be transmitted to the processor; and

transmitting an early data ready indication to a processor to drain a request seeking the data from a resource scheduler.

11. The method of claim 10, further comprising:

transmitting a data ready indication to the processor when the data is ready; and

filling a first level cache (FLC) of a data cache coupled with an execution unit.

12. The method of claim 10, wherein the detecting of the readiness of the data is performed by a memory controller.

13. The method of claim 10, wherein the transmitting of the early data ready indication is performed by the memory controller via a bus interface unit, the memory controller coupled with the bus interface unit via a front side bus.

14. An apparatus, comprising:

a processor having a resource scheduler having one or more requests waiting for data to be loaded into a data cache including a first level cache (FLC); and

a memory controller coupled with the processor, the memory controller having an early data ready mechanism to detect readiness of the data one or more bus clocks prior to data being ready to be transmitted to the processor, and transmitting an early data ready indication to the processor to drain the one or more requests from the resource scheduler.

15. The apparatus of claim 14, wherein the processor further comprises a bus interface unit to receive the transmitted early data ready indication from the memory controller and to transmit the early data ready indication to the resource scheduler having a rescheduled request queue (RRQ).

16. The apparatus of claim 15, wherein the bus interface unit is coupled with the memory controller via a front side bus.

17. The apparatus of claim 14, wherein the processor further comprising:

an instruction queue to receive the one or more requests from one or more instruction sources;

one or more schedulers to schedule the one or more requests and to pass the one or more requests on to an execution unit having the data cache;

a replay controller/checker (replay checker) to check contents of the data cache

and to replay the one or more requests if the data is not located in the data cache; and

a reorder buffer to store the one or more requests that are replay safe.

18. The apparatus of claim 14, wherein the data cache further comprises a second level cache (SLC).

19. A system, comprising:

a storage medium;

a processor coupled with the storage medium, the processor having resource scheduler having one or more requests waiting for data be loaded into a data cache including a first level cache (FLC), and

a memory controller coupled with the processor, the memory controller having an early data ready mechanism to detect readiness of the data one or more bus clocks prior to data being ready to be retrieved from memory, and transmitting an early data ready indication to the processor to drain the one or more requests from the resource scheduler.

20. The system of claim 19, wherein the processor further comprises a bus interface unit to receive the transmitted early data ready indication from the memory controller and to transmit the early data ready indication to the resource scheduler having a rescheduled request queue (RRQ).

21. The system of claim 20, wherein the bus interface unit is coupled with the memory controller via a front side bus.

22. The system of claim 19, wherein the processor further comprising:

an instruction queue to receive the one or more requests from one or more

instruction sources;

one or more schedulers to schedule the one or more requests and to pass the one or more requests on to an execution unit having the data cache;

a replay controller/checker (replay checker) to check contents of the data cache and to replay the one or more requests if the data is not located in the data cache; and

a reorder buffer to store the one or more requests that are replay safe.

23. A machine-readable medium having stored thereon data representing sets of instructions, the sets of instructions which, when executed by a machine, cause the machine to:

access data cache for data in response to a request for the data, the request received from an instruction source;

wait for the data to be retrieved from memory if the data is not located in the data cache; and

receive an early data ready indication at a resource scheduler the early data ready indication being received prior to receiving a data ready indication referring to the data being ready to be retrieved from the memory.

24. The machine-readable medium of claim 23, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

receive the data ready indication; and

fill the data cache with the data.

25. The machine-readable medium of claim 23, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

insert the request into the resource scheduler if the data is not located in the data cache; and

save the request in the resource scheduler to wait for the data to be retrieved from the memory.

26. The machine-readable medium of claim 24, wherein the sets of instructions which, when executed by the machine, further cause the machine to:

access the data cache with the request while the data cache is being filled with the data; and

meet the request with the data from the data cache.

27. The machine-readable medium of claim 23, wherein the resource scheduler is coupled with a bus interface unit to receive the early data ready indication from a memory controller, the resource scheduler having a rescheduled request queue (RRQ).

28. A machine-readable medium having stored thereon data representing sequences of instructions, the sequencing of instructions which, when executed by a machine, cause the machine to:

detect readiness of data one or more bus clocks prior to data being ready to be retrieved from memory; and

transmit an early data ready indication to a processor to drain a request seeking the data from a resource scheduler.

29. The machine-readable medium of claim 28, wherein the sequences of instructions which, when executed by the machine, further cause the machine to:

transmit a data ready indication to the processor when the data is ready; and

fill a data cache with the data, the data cache comprising a first level cache (FLC) coupled with an execution unit.

30. The machine-readable medium of claim 28, wherein the transmitting of the early data ready indication is performed by a memory controller via a bus interface unit, the memory controller coupled with the bus interface unit via a front side bus.